

Scalable Planar Trapology

- Introduction
 - Scaling with vertical interconnects
 - Planar traps using VLSI fabrication
 - Design
 - Fabrication
 - Ion heating in planar traps
 - Thermal noise
 - RF source noise
 - Anomalous noise
 - Present status
 - Initial traps
 - RF performance
 - Revised traps
 - ✓ Linear
 - ✓ X trap
 - Interface to ion groups
 - Ion loading
 - Through laser beam access
- Dick Slusher
Bell Labs
Lucent Technologies



Collaborators

Bell Labs:

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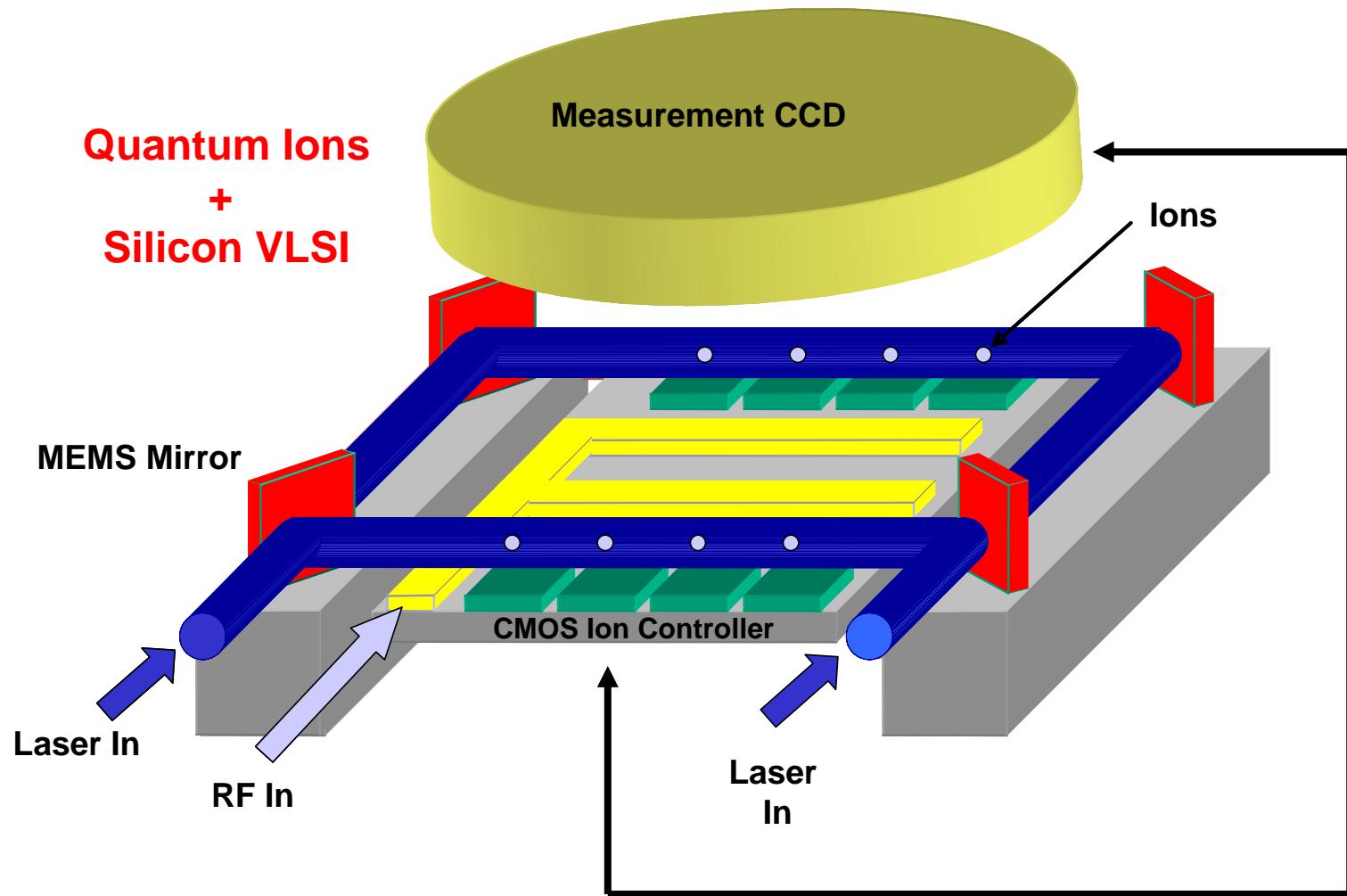
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Rainer Reichle

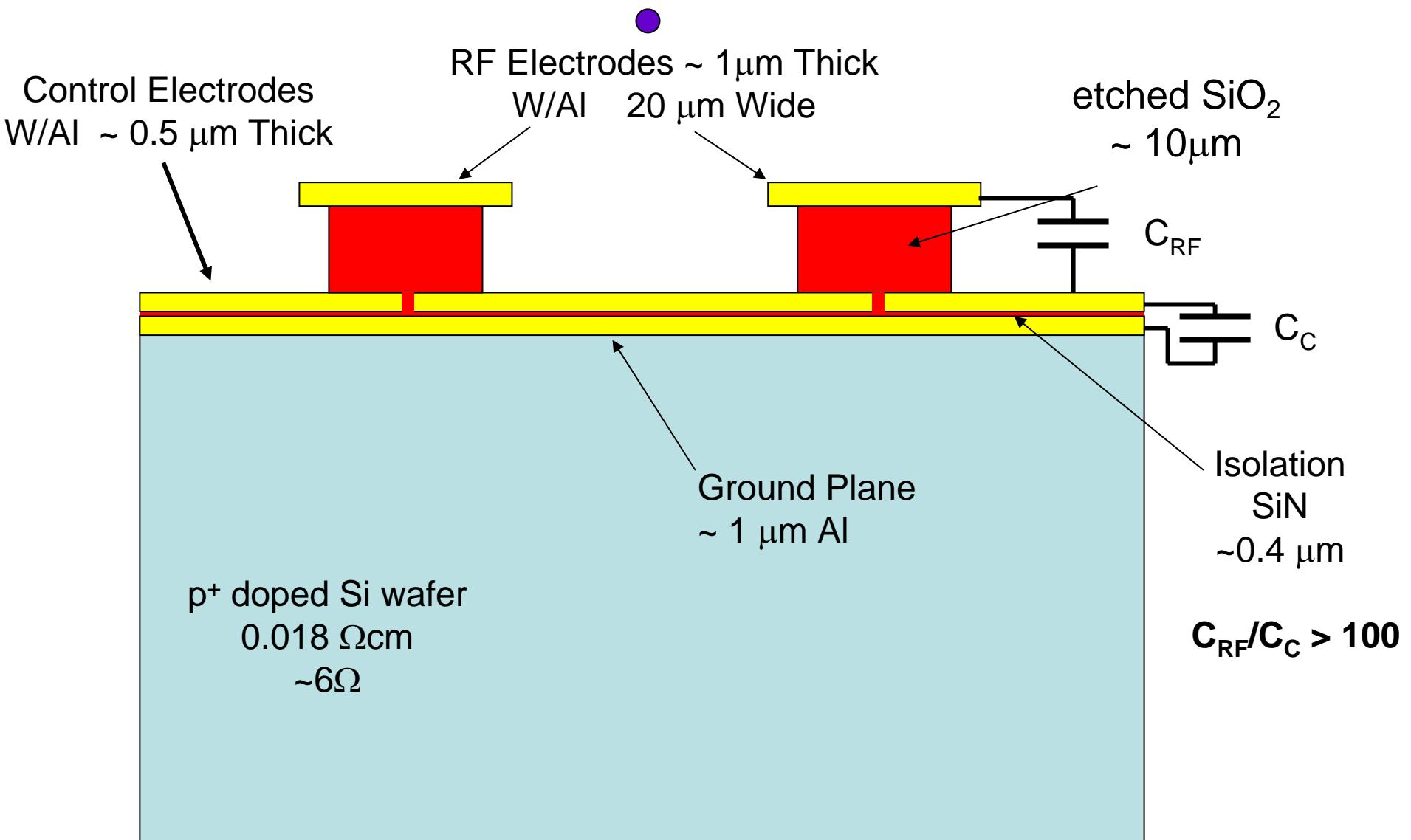
Scalable Ion Trap Quantum Computer Vision



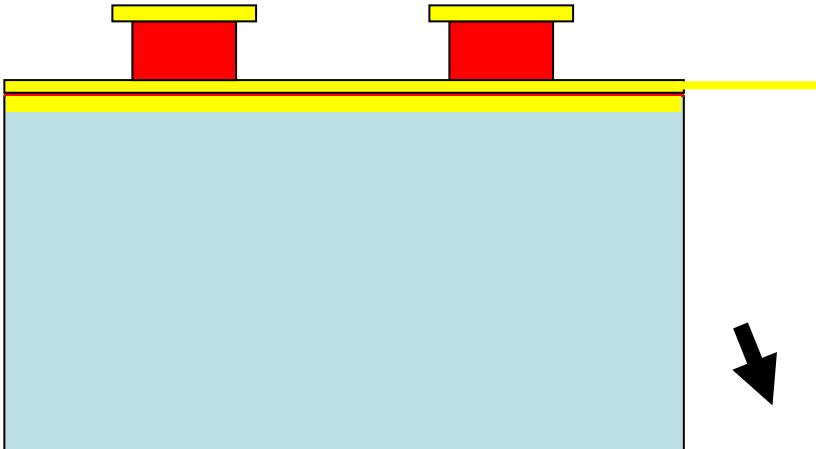
System Compatibility of Quantum & Classical: Spatial Pitch, Clock Speed
Operating Temperature, Power Dissipation

Planar Ion Trap

Scalable Silicon VLSI

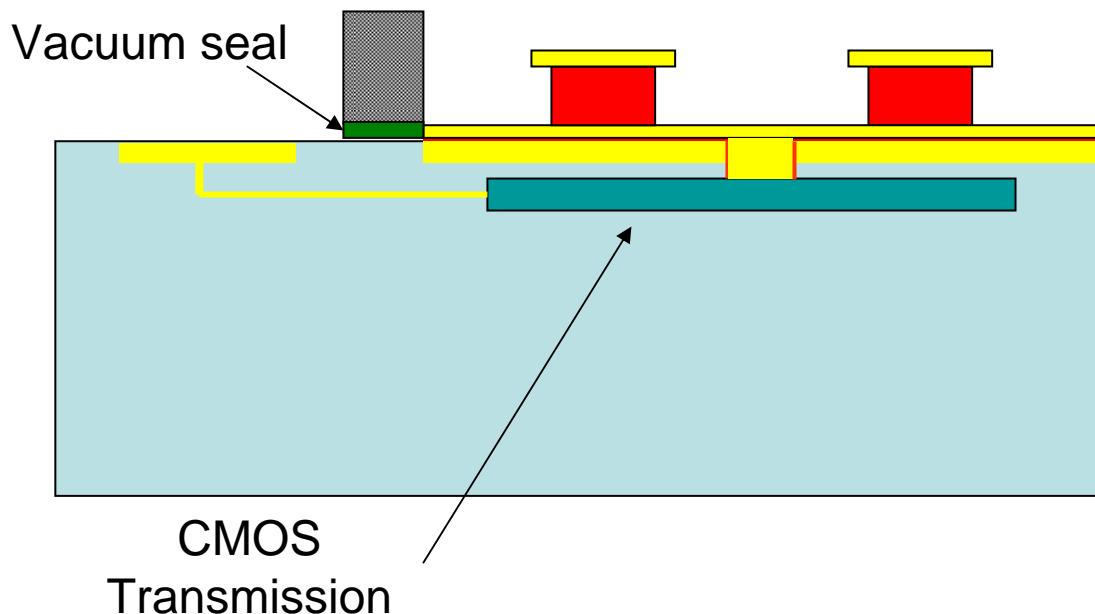


Evolution Path



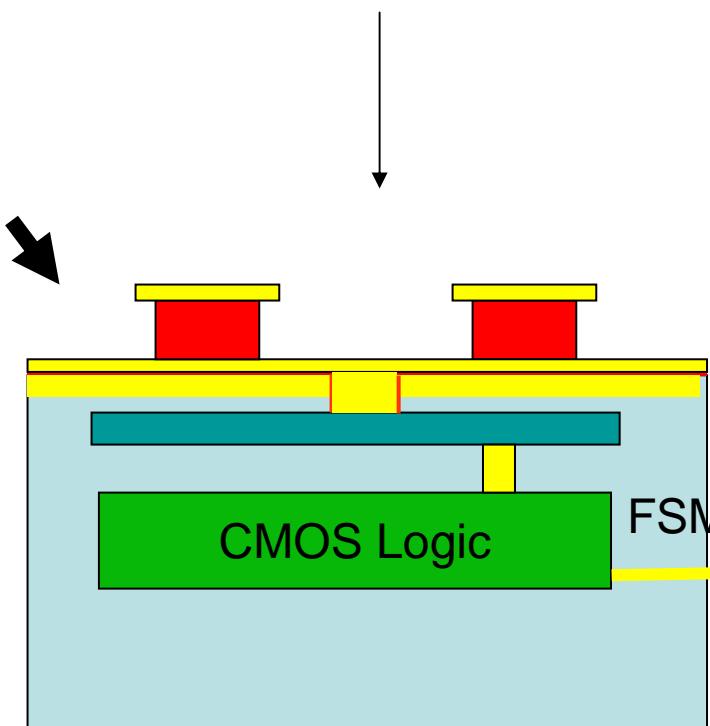
Digital Analog Voltage (DAC) source

Dramatic reduction in interconnect density with vertical Interconnects and CMOS electronics
~ 1000 ion/cm²

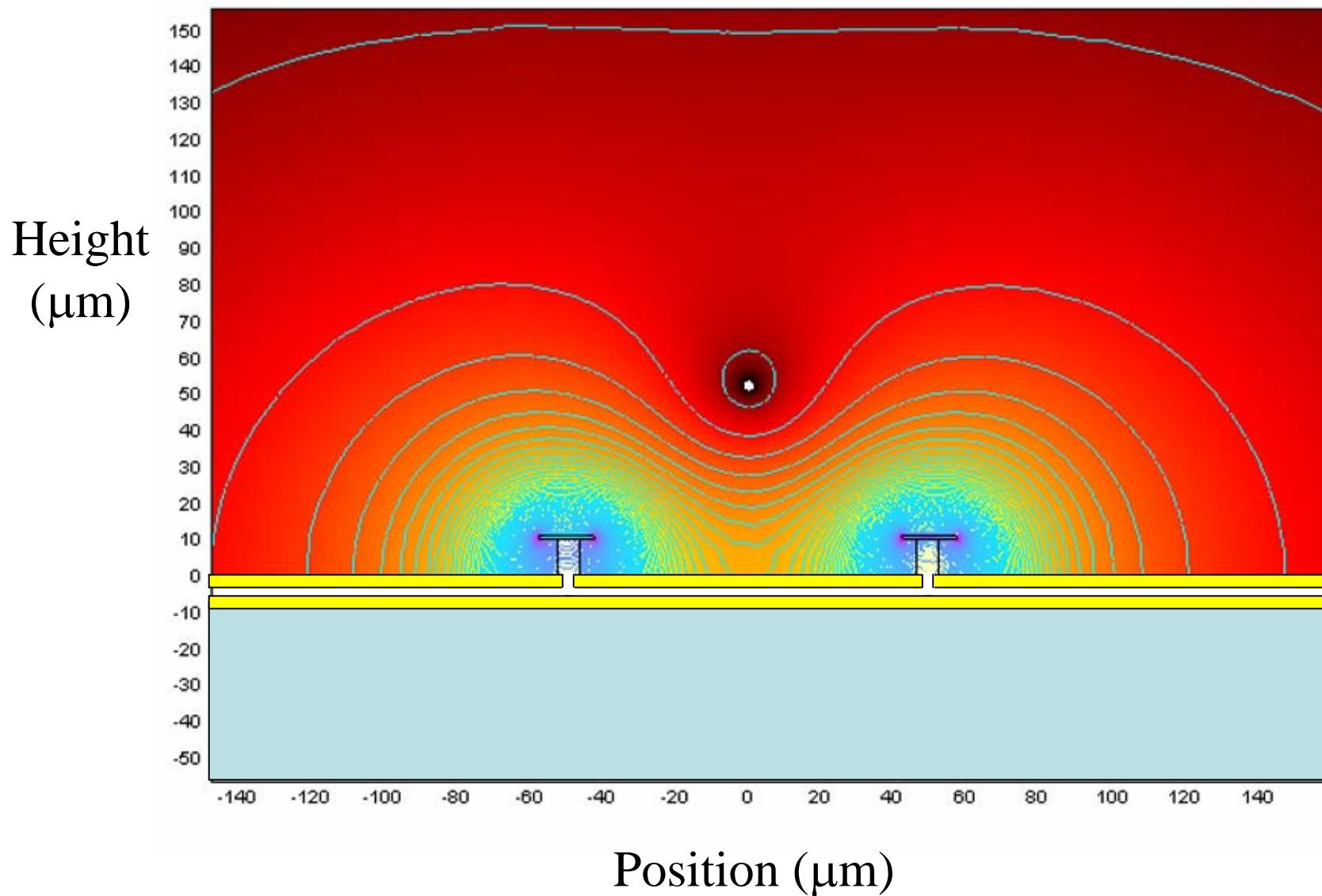


CMOS
Transmission
gate
switch

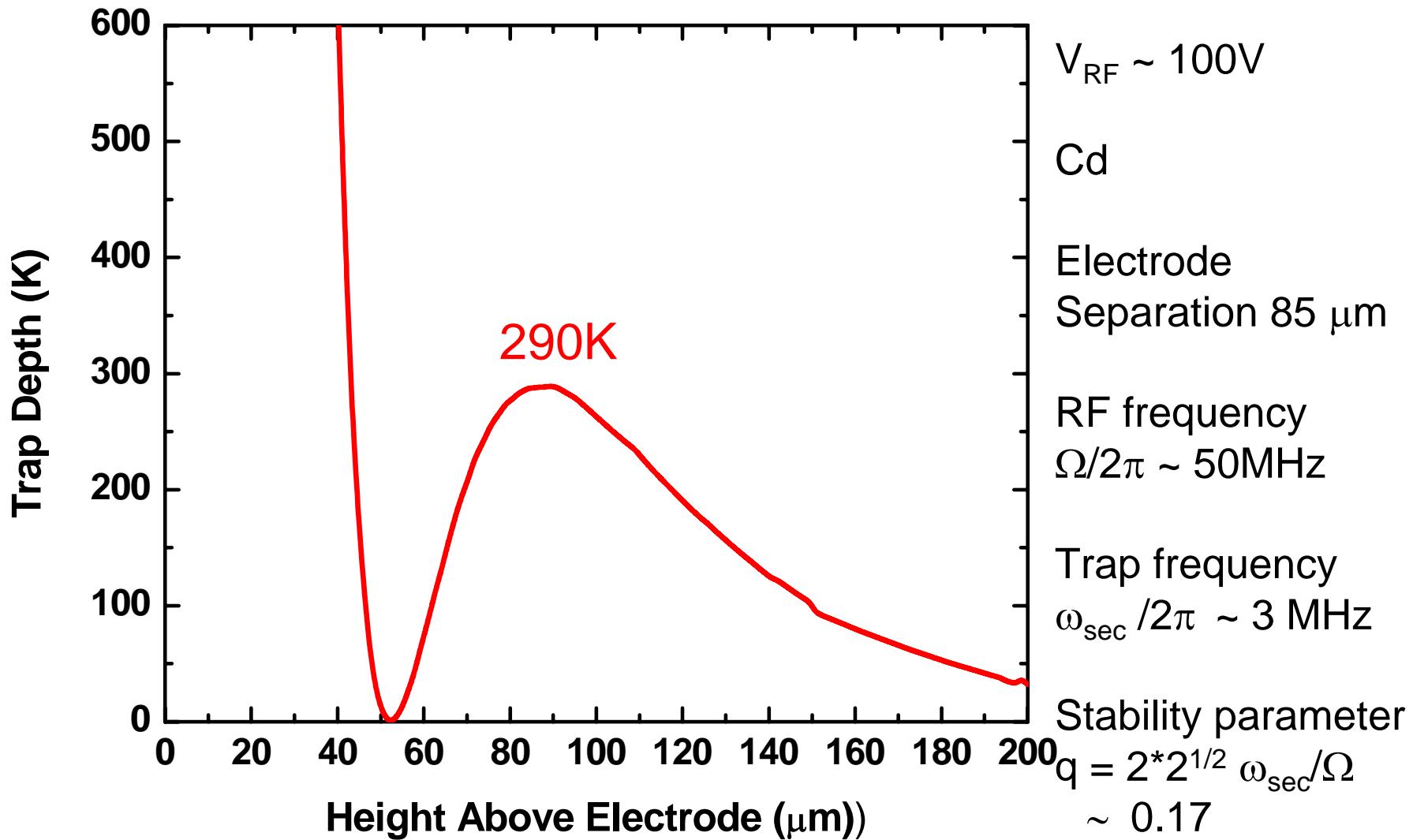
Monolithic integration
allowed by low T trap fabrication



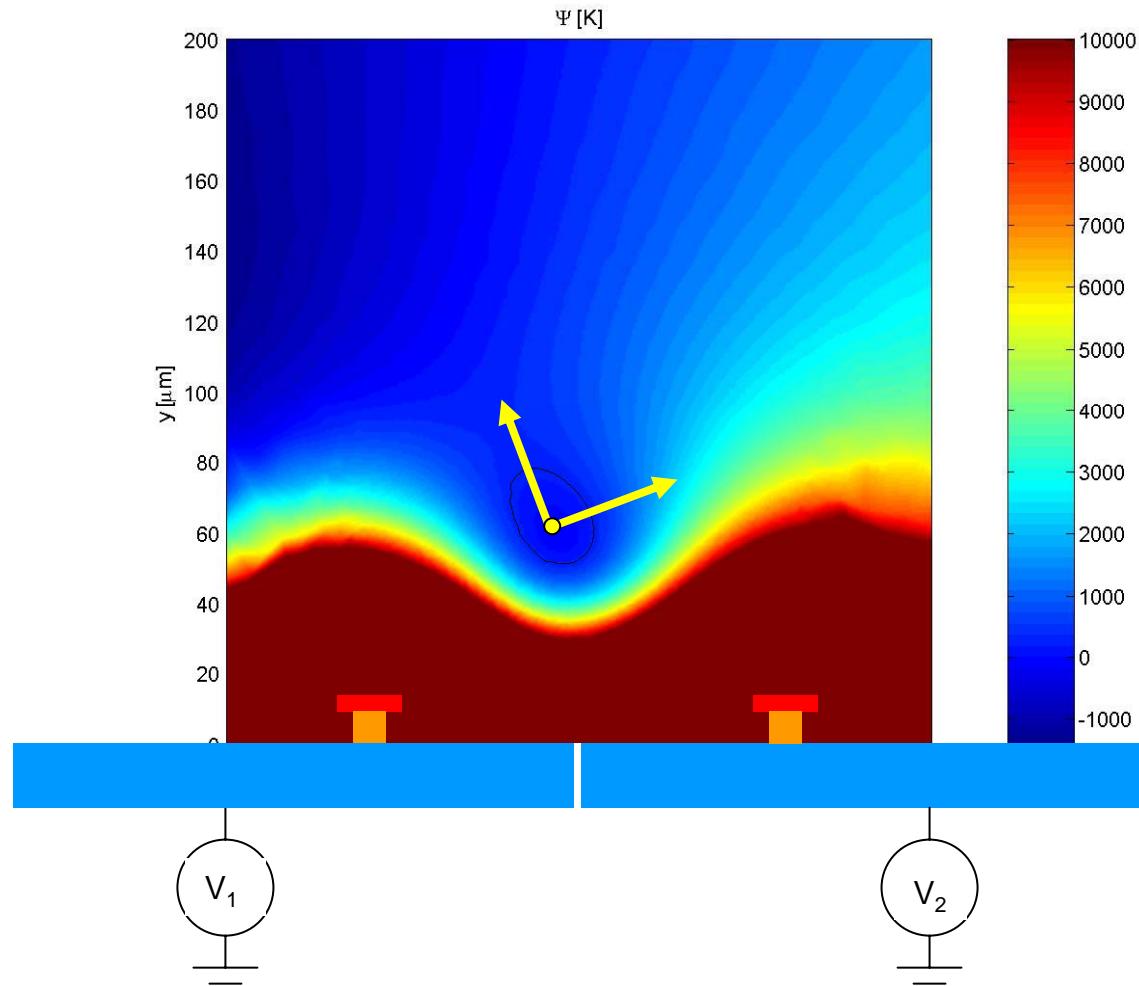
Electric Fields Above Scalable Ion Trap



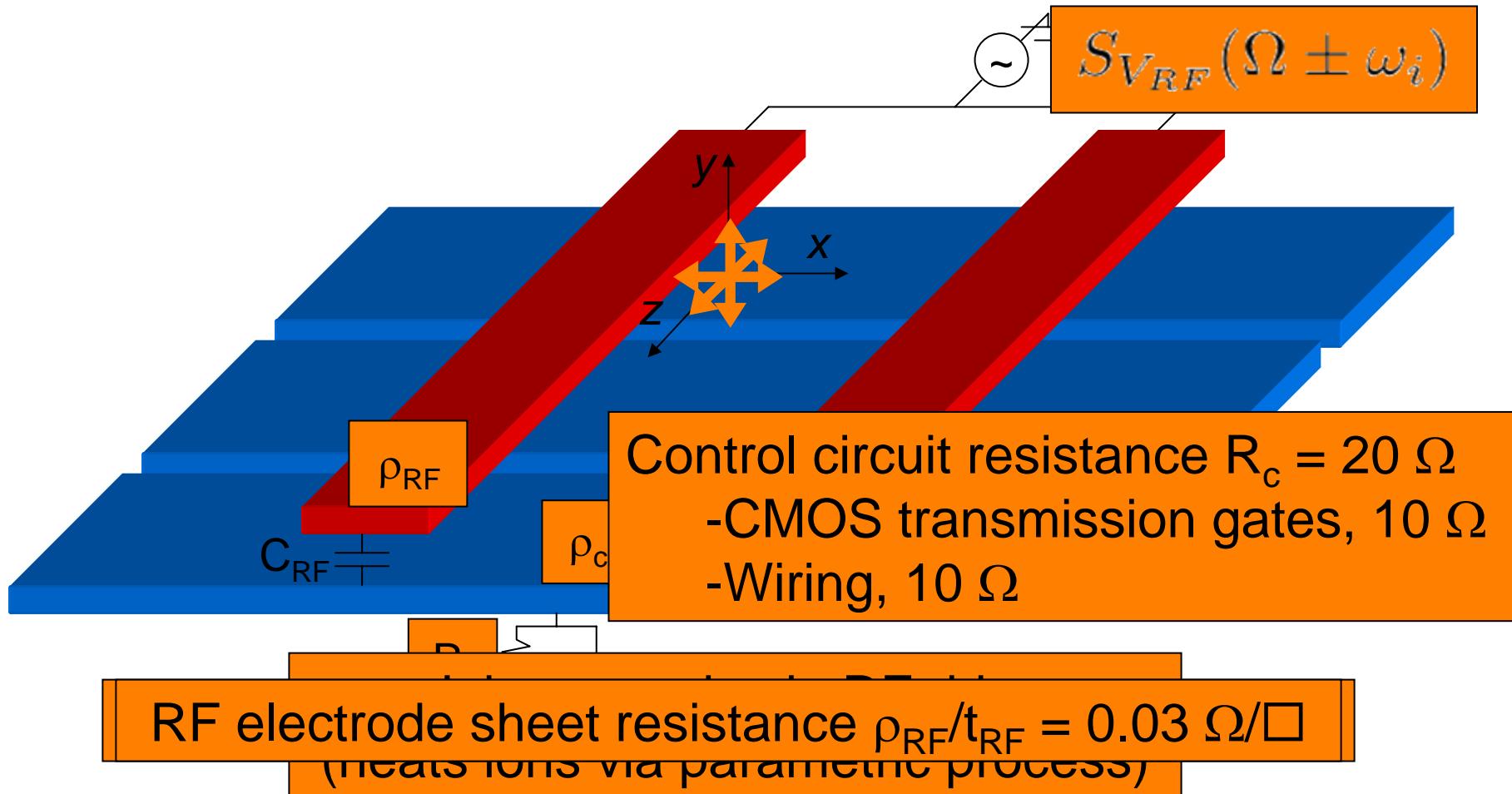
Trap Loading Problems?



Split control electrodes for doppler cooling

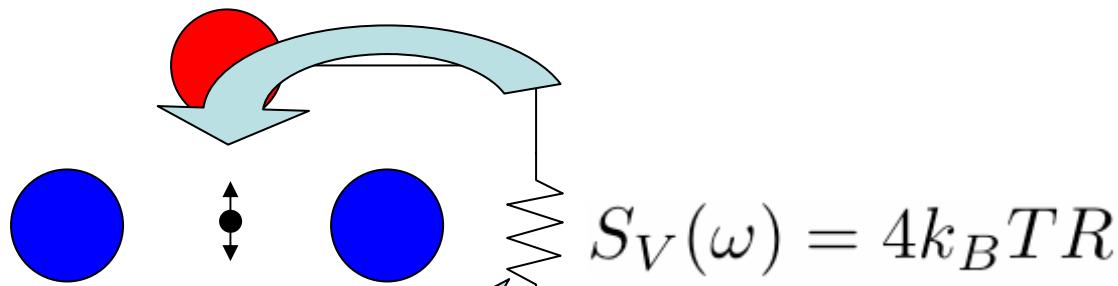


Sources of Johnson noise heating in planar traps

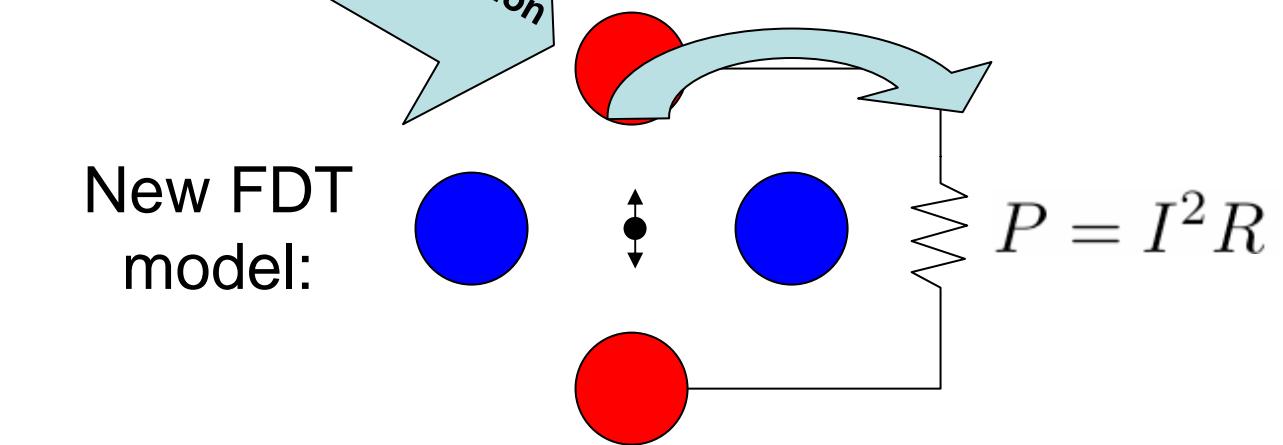


Johnson noise ion heating

Standard
model:



New FDT
model:



Definitions

- Heating rate:

$$\dot{n} = \frac{Q^2}{4m\hbar\omega} S_E(\omega) \sim 100 \text{ s}^{-1}$$

- Figure of merit:

$$F = \frac{1}{\dot{n}\tau_2} \sim 1000$$

$\tau_2 = 2$ qubit gate time $\sim 10 \mu\text{sec}$

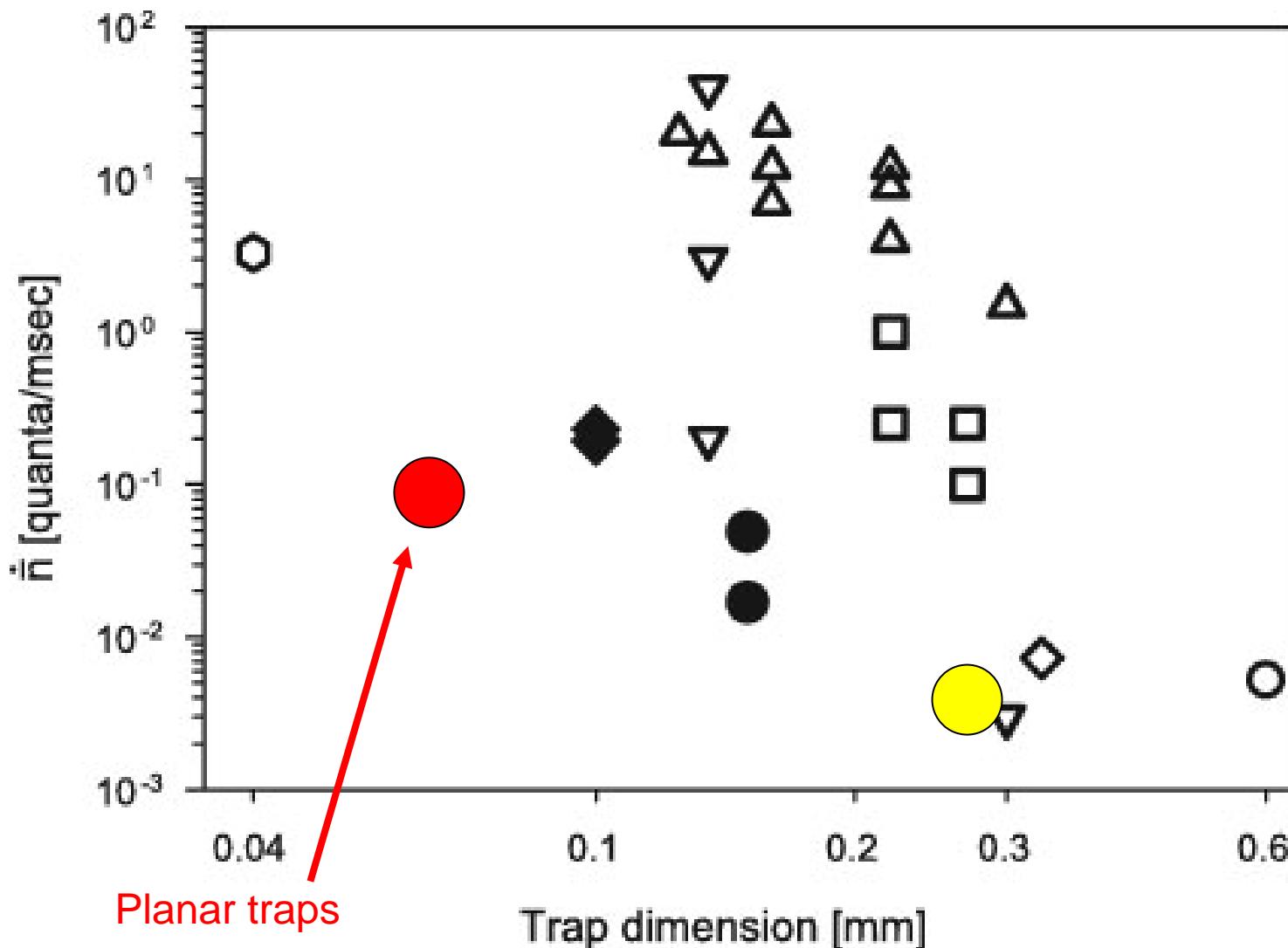
Johnson noise heating rates

	\dot{n}_x [s ⁻¹]	\dot{n}_y [s ⁻¹]	\dot{n}_z [s ⁻¹]
R _c	-	480	170
ρ_c	0.37	0.37	0.73
ρ_{RF}	8.0	0.57	-
$S_{VRF}(\Omega \pm \omega_i)$	-	0.2	-
Total	8.4	480	170



$F \sim 500$

Ion Heating Experiments



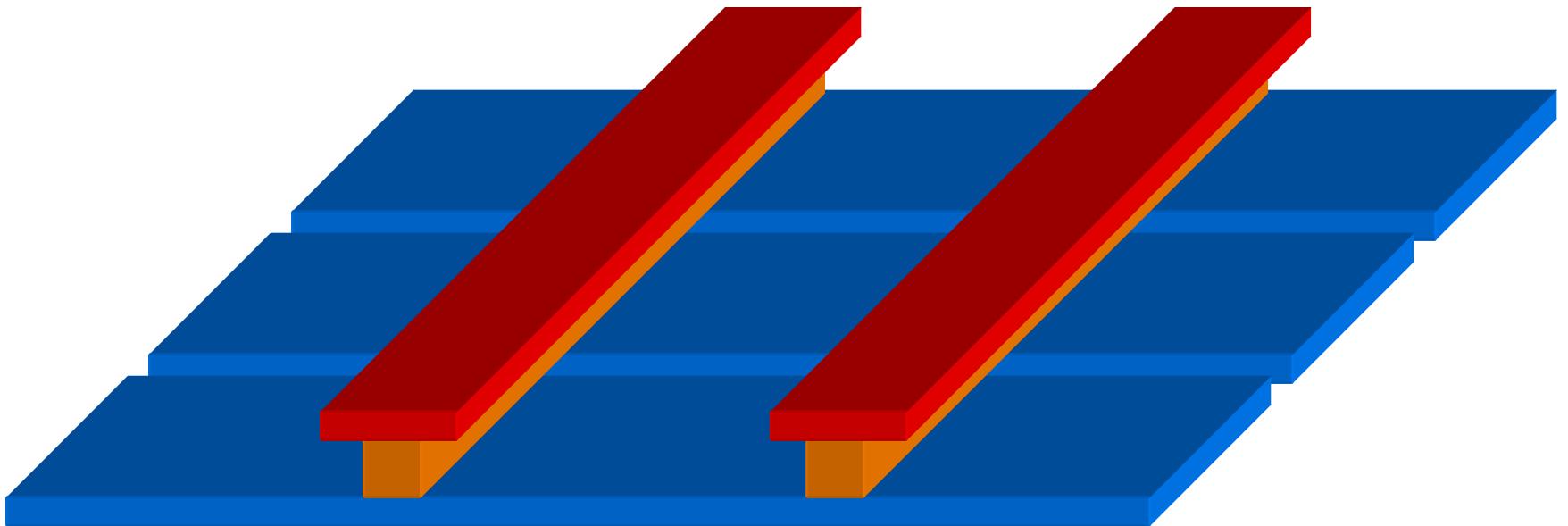
Anomalous heating rates

- Current experiments see heating rates 10 to 100 times larger than Johnson noise
- Scaling from current experiments to the planar traps predicts an anomalous heating rate between 10^4 and 10^5 s^{-1}

$$\rightarrow F \sim 10$$

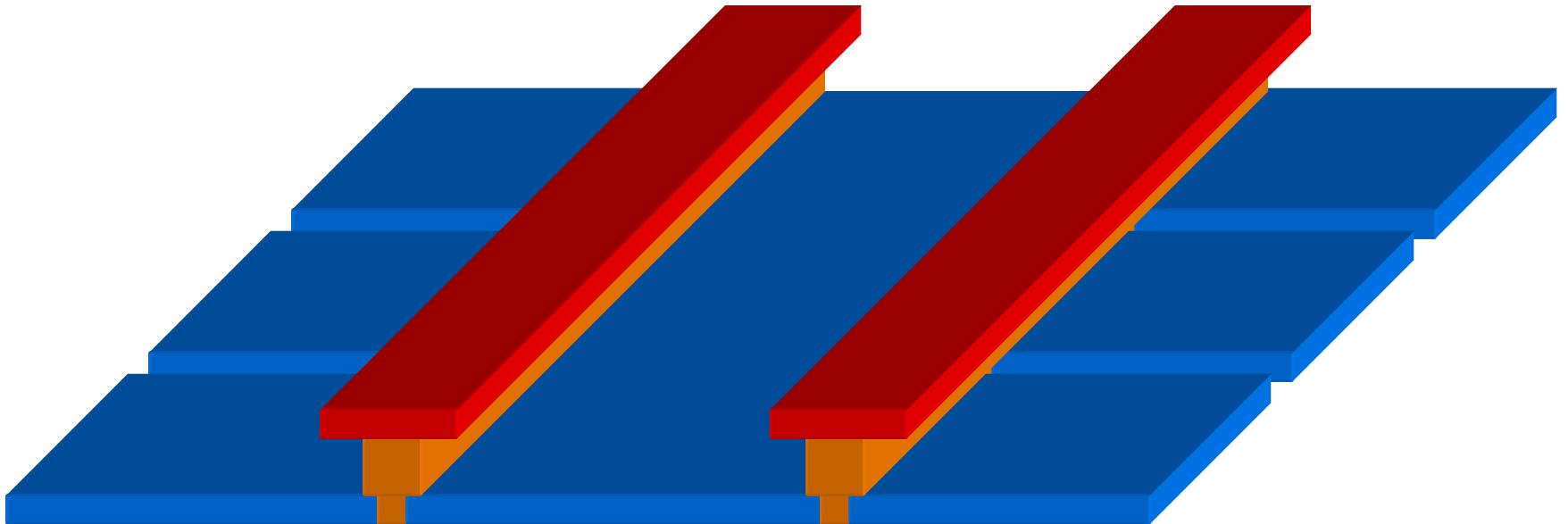
- What causes this anomalous heating?
 - Grain boundaries (too slow?)
 - Charging dynamics between grains or grain clusters
 - Surface roughness (can enhance fields)
 - Metal deposited on electrodes by ion source
 - Moving atoms or ledges (Au worst)

First generation control electrode layout

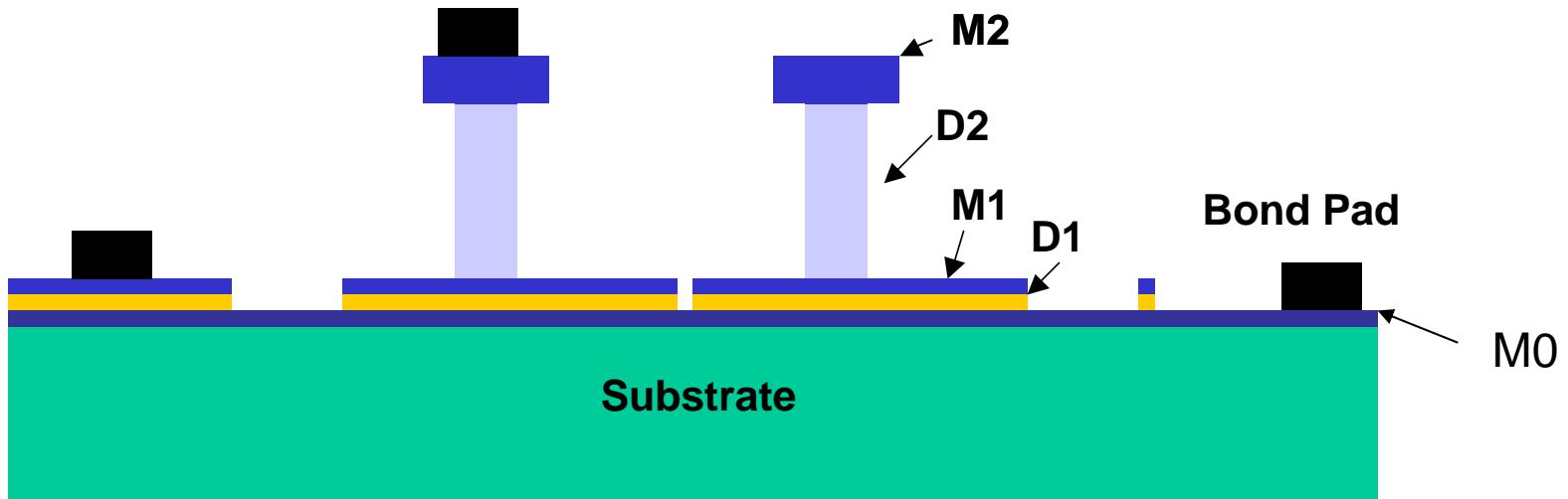


New control electrode layout

- Eliminating split between RF electrodes reduces z Johnson noise heating by a factor of 5
- Cooling and micro-motion control



Fabrication and Materials



- Substrate:
p-type (resistivity 0.018 ohm-cm)
- Dielectric D1:
Nitride: 4000A, k ~ 7.5
- Metal M0 & M1:
Al (4500A) /W (600A) : (0.06 ohm/sq)
- Dielectric D2:
Oxide: 10 um PETEOS, stress balanced
- Metal M2:
Al (9400A) /W (600A): (0.031 ohm/sq)

Linear Ion Trap Layout

Version 1.0.0

Wirebond pads for control electrodes

RF input lines are 72 μm wide,

They split into trapping electrodes that are spaced by:

40 μm (18-21) control electrodes

60 μm (14-18)

80 μm (9-14)

100 μm (4-9)

120 μm (1-4)

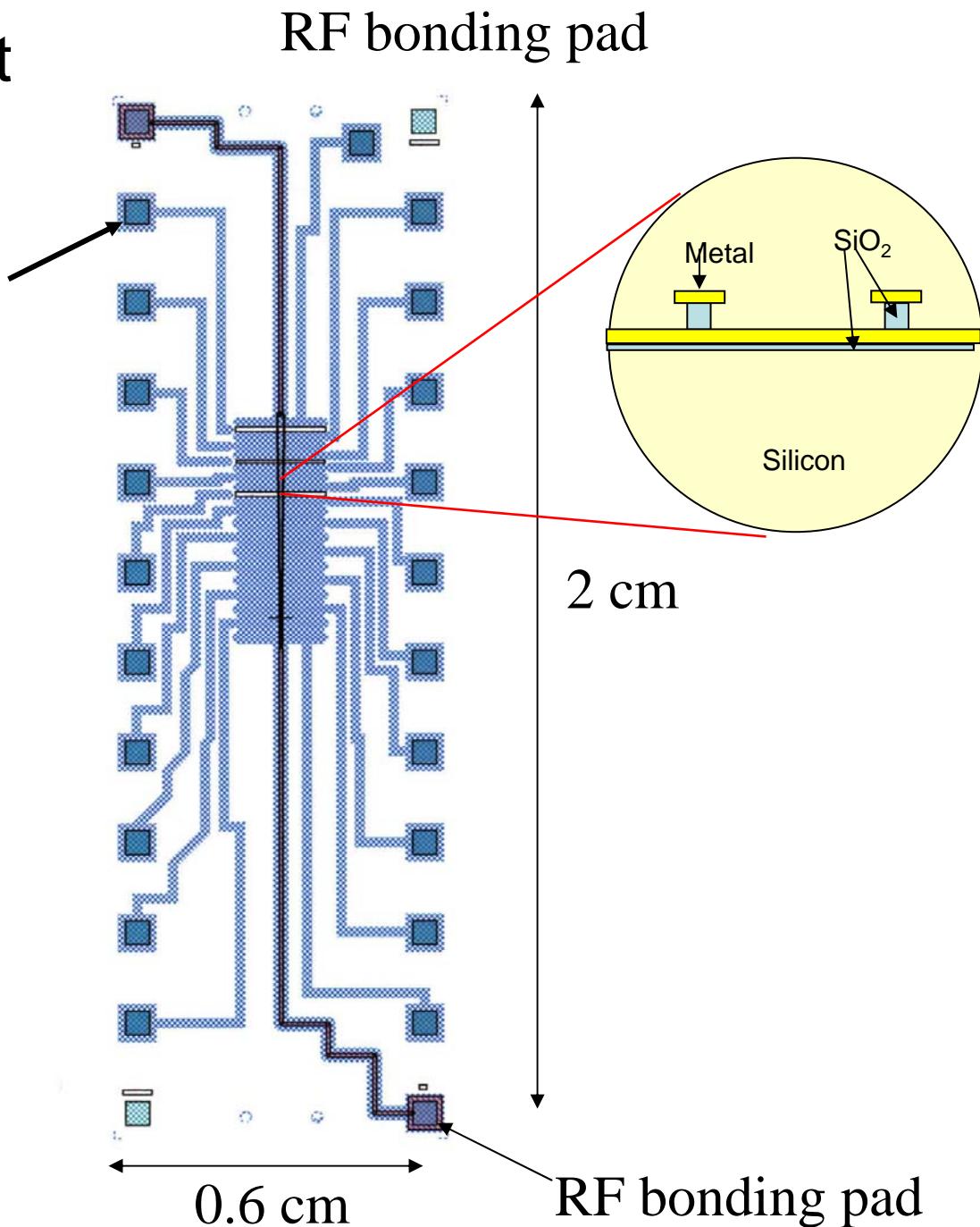
Control electrodes are 2 mm wide and have lengths(in μm):

(sequence starts at the top)

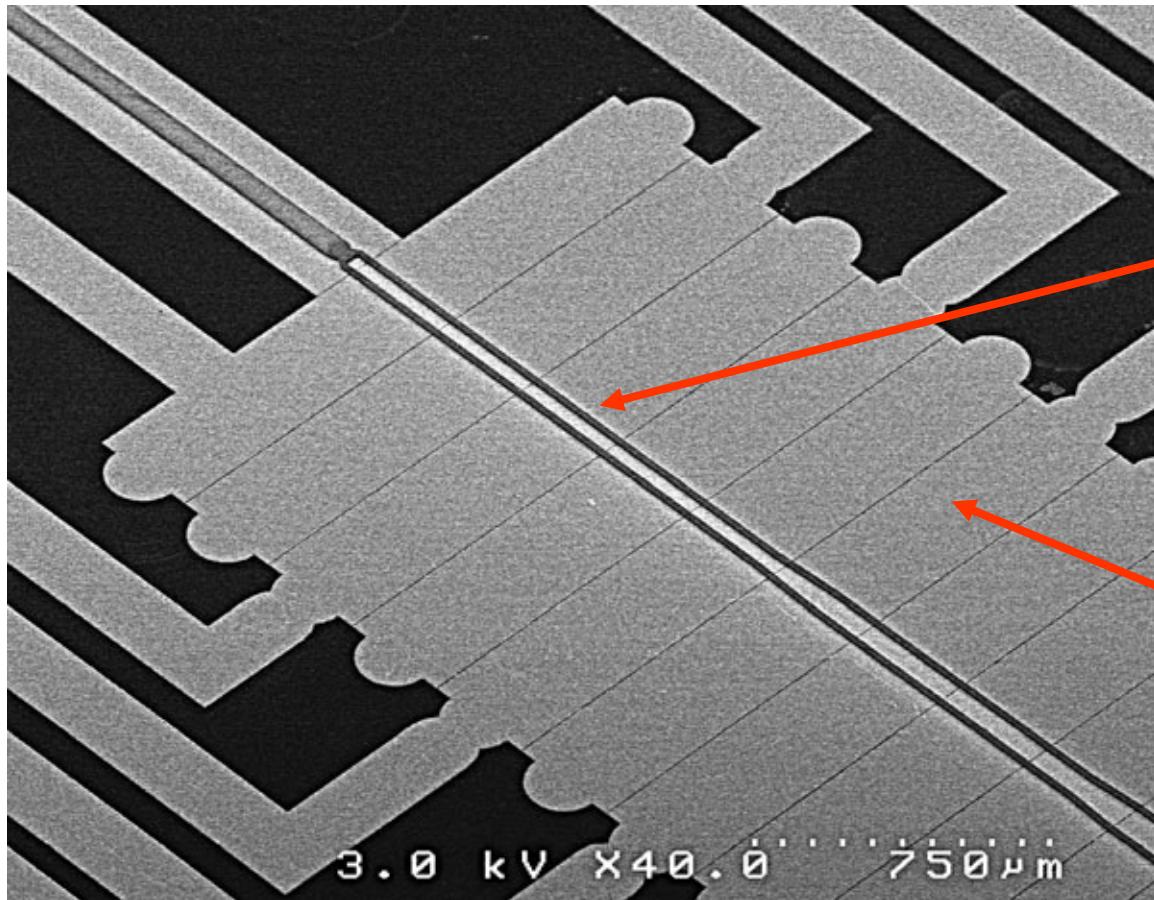
200,100,200,200,200,50,200,

200,200,100,200,200,300,300,

300,300,300,300,300,300,300.

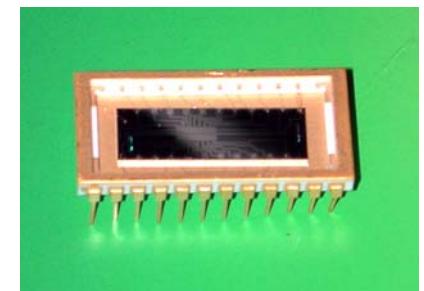


Initial Trap SEM Image



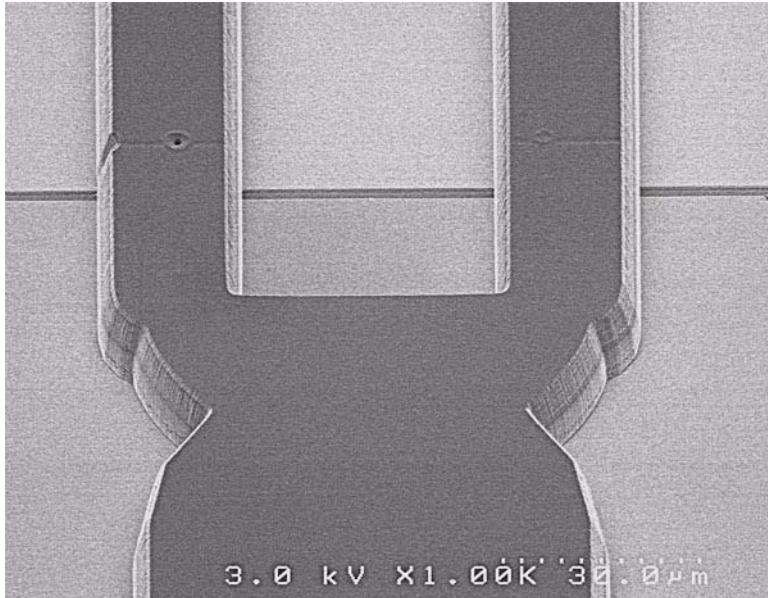
RF electrodes

Control electrodes

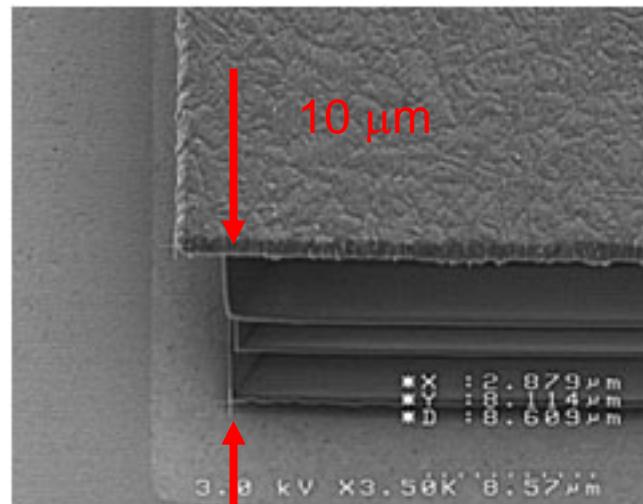
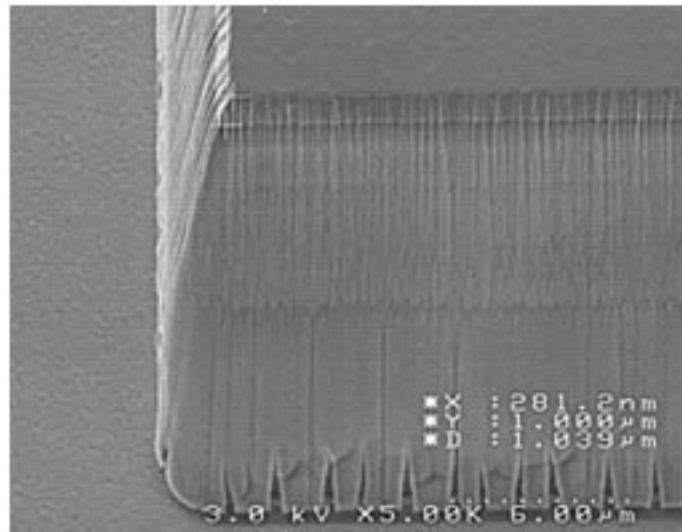
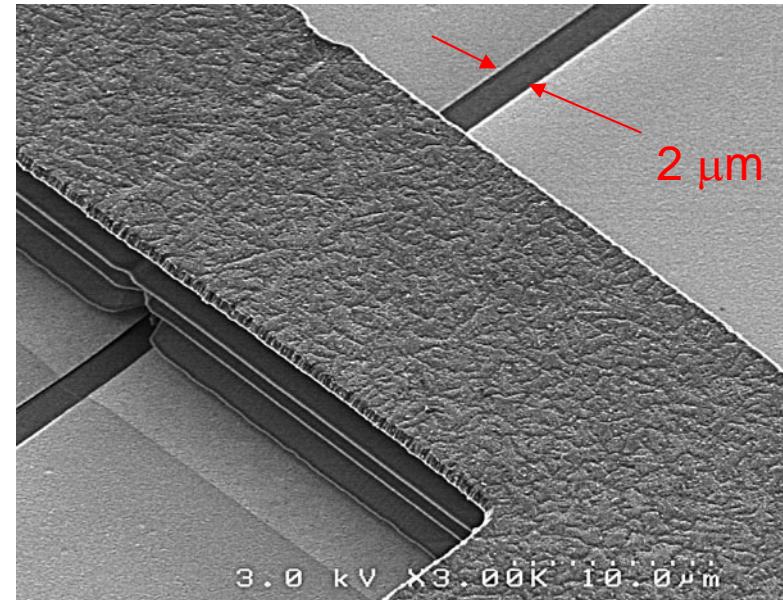


RF Electrode SEMs

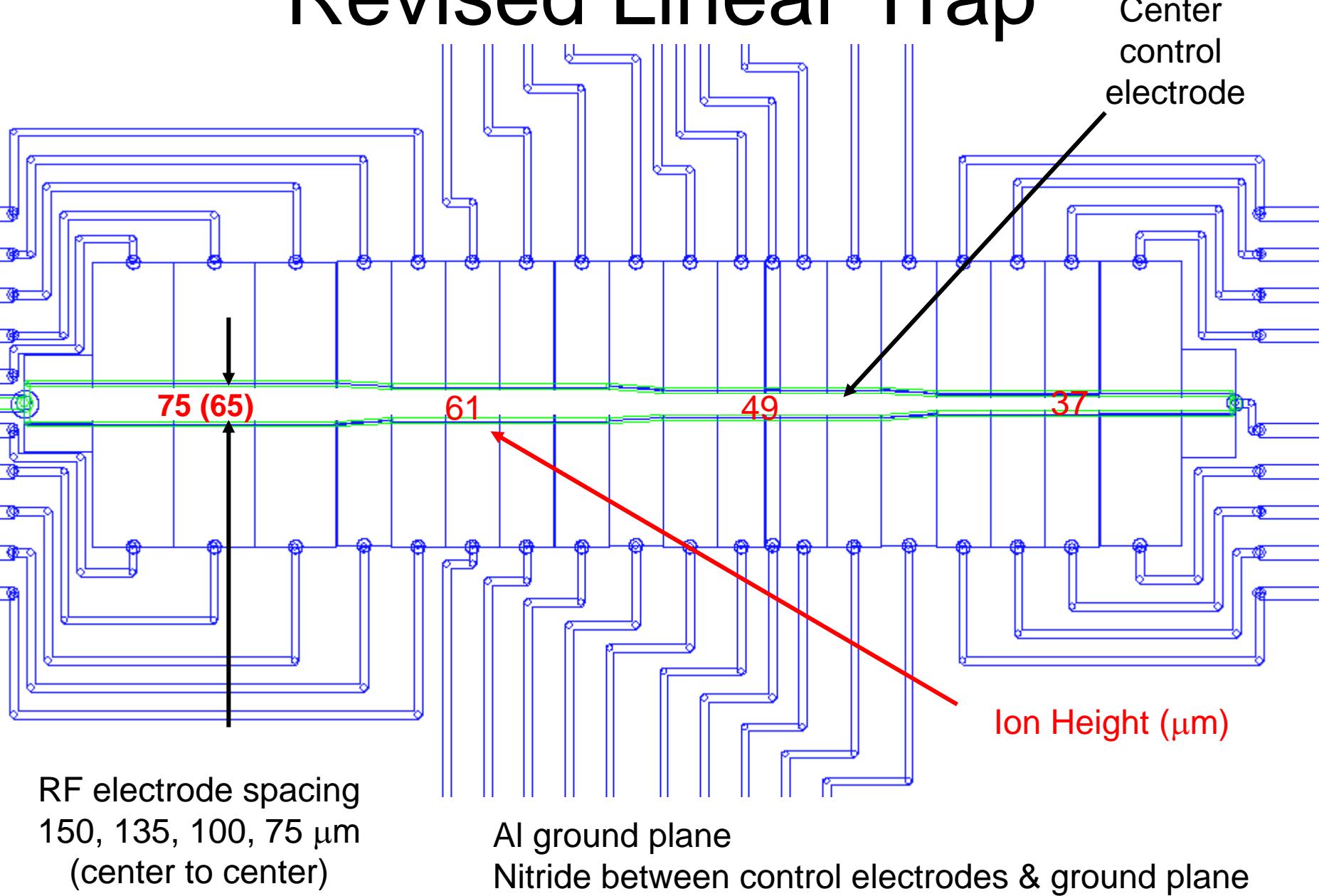
After dry etch/before wet etch



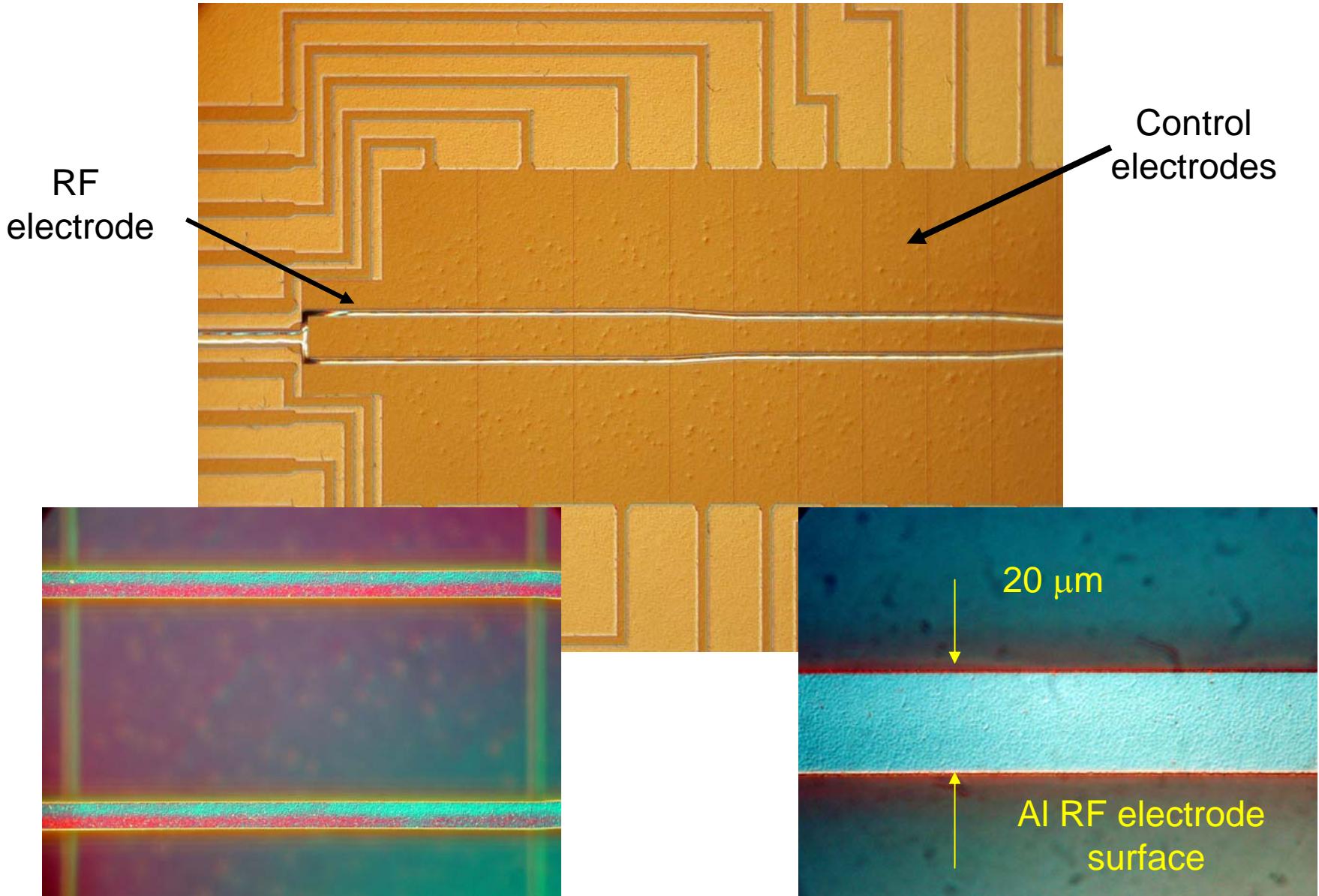
After wet etch with electrode under-etch



Revised Linear Trap



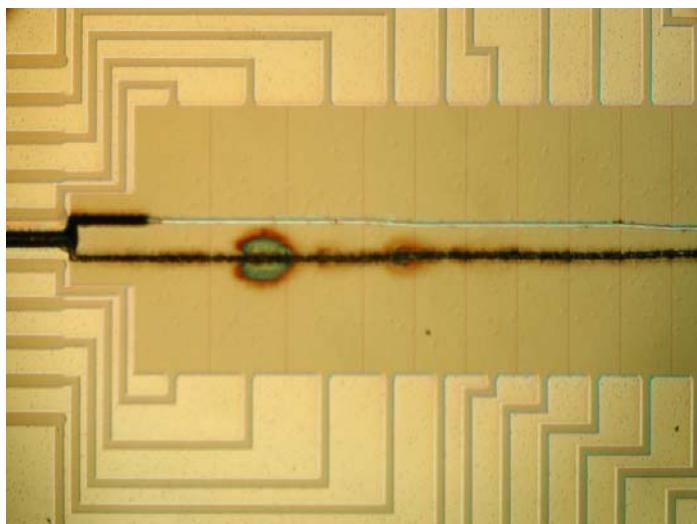
Revised Linear Trap



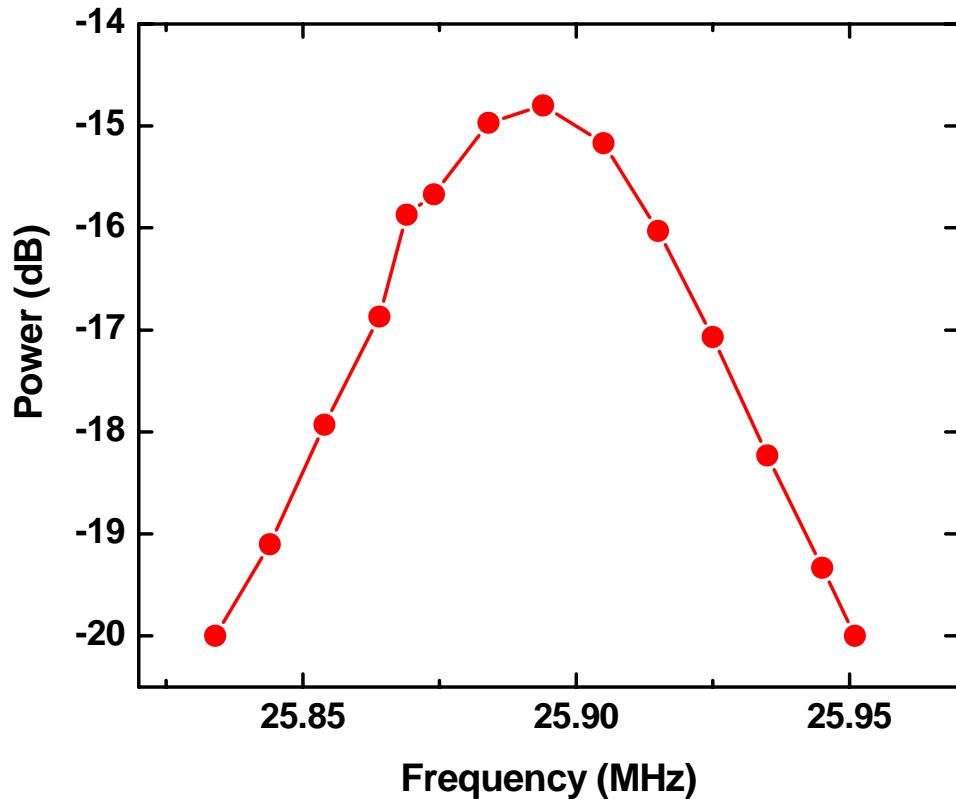
RF Drive

Capacitance $\sim 4.6 \text{ pf}$
Loss tangent ~ 0.0025

Limit RF voltage $\sim 400 \text{ V peak}$
(in air)
 $>300 \text{ V}$ (in vacuum)
➤ Outgassing



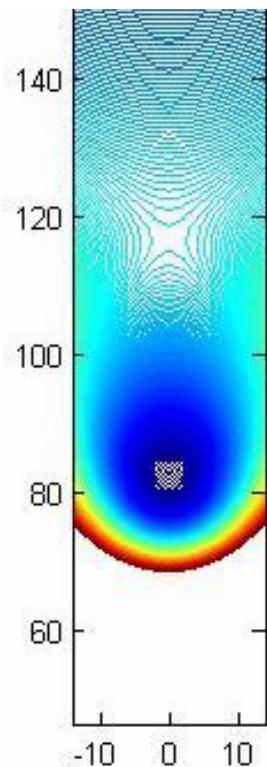
Breakdown at 500 V peak



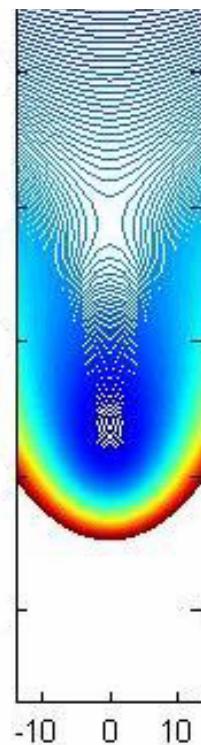
$Q \sim 360$

Planar Cross Problem

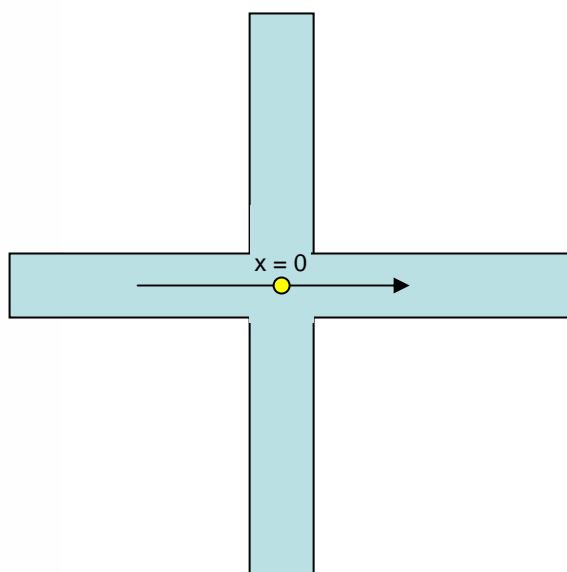
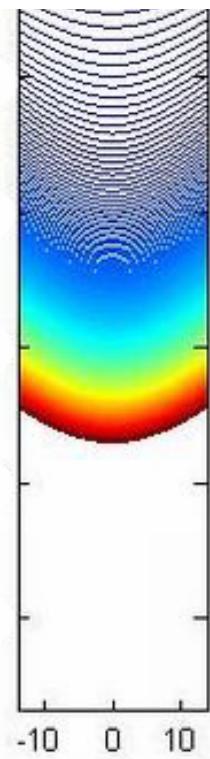
$x = -140 \mu\text{m}$



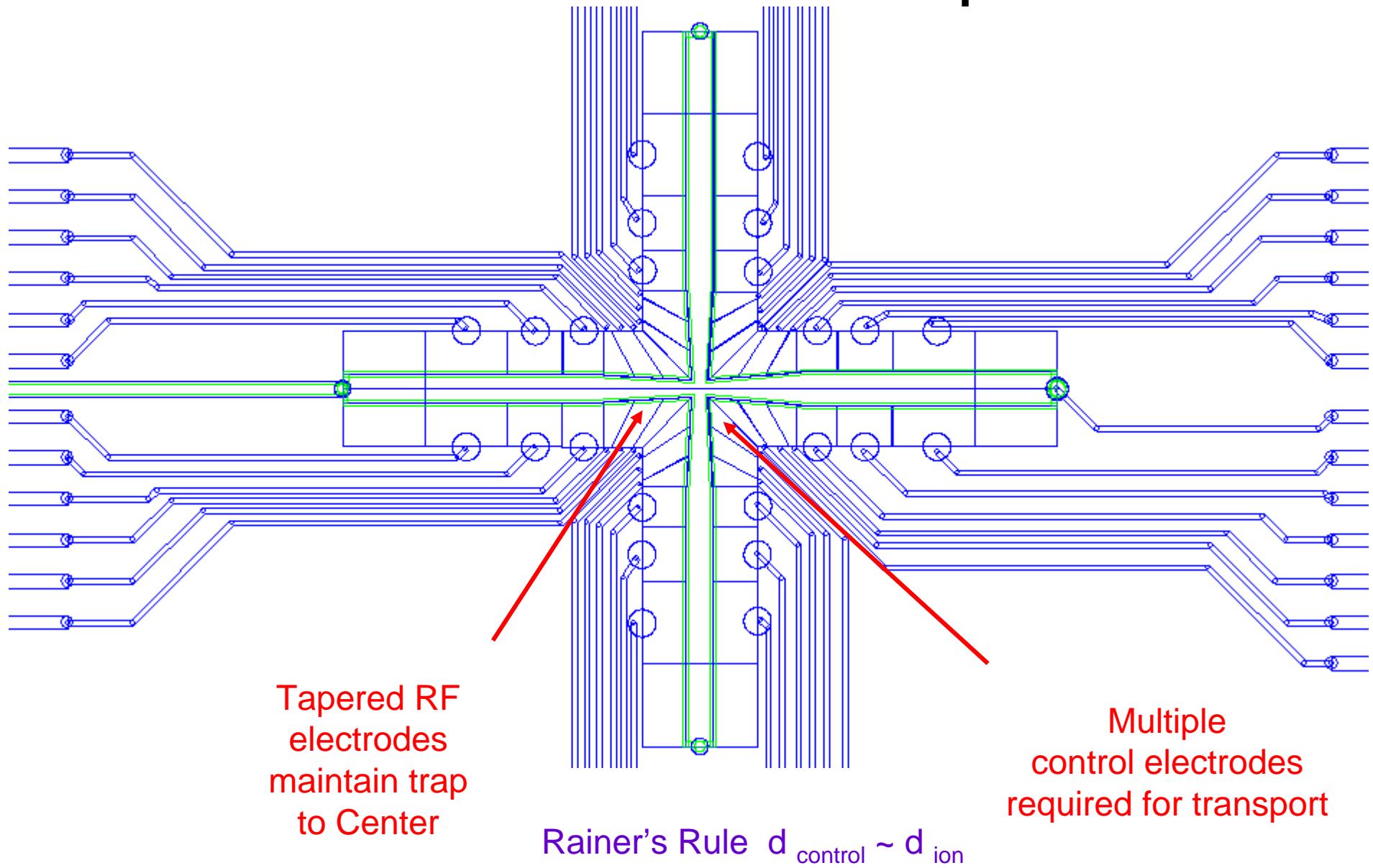
$x = -110 \mu\text{m}$



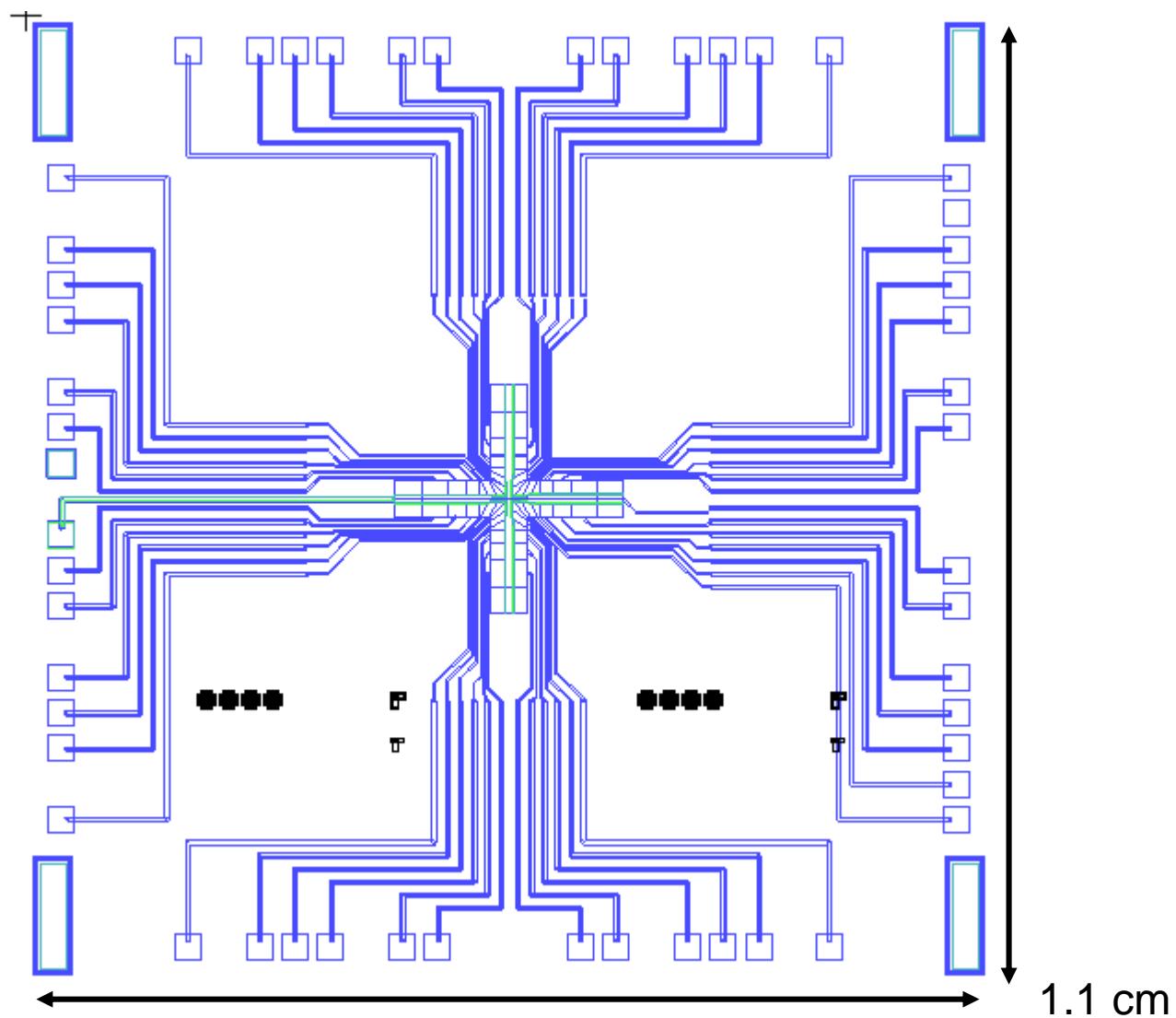
$x = -75 \mu\text{m}$



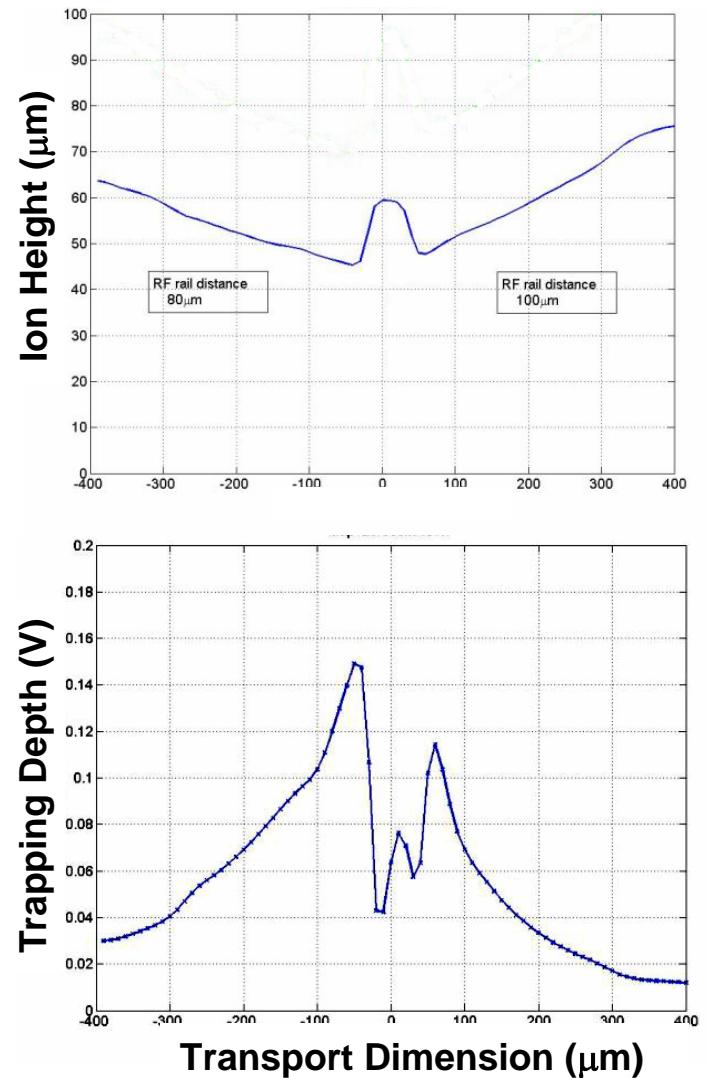
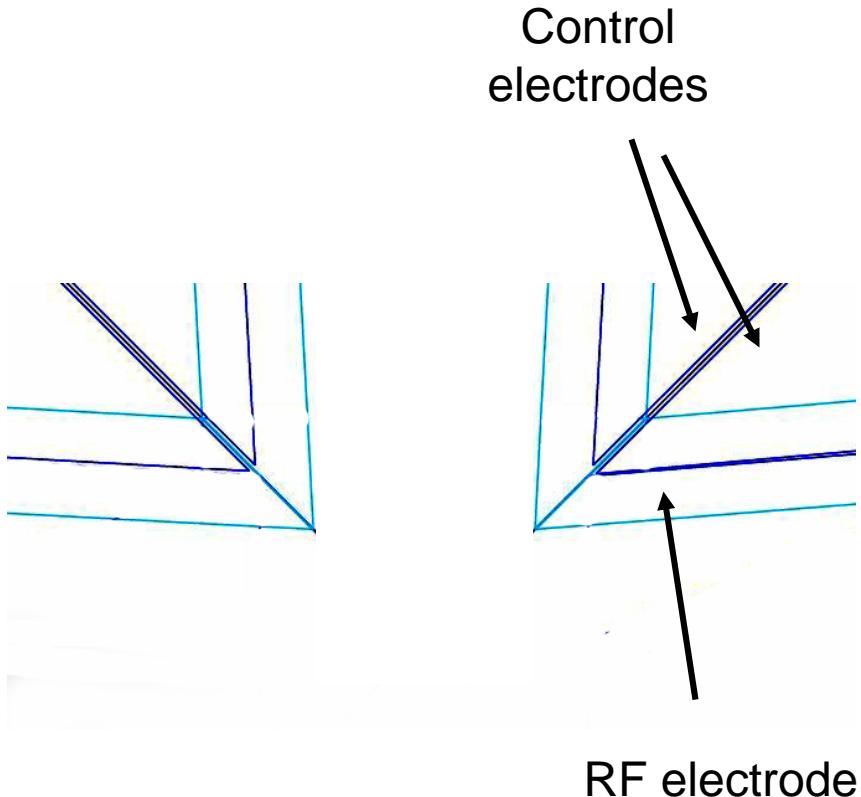
Cross Planar Trap



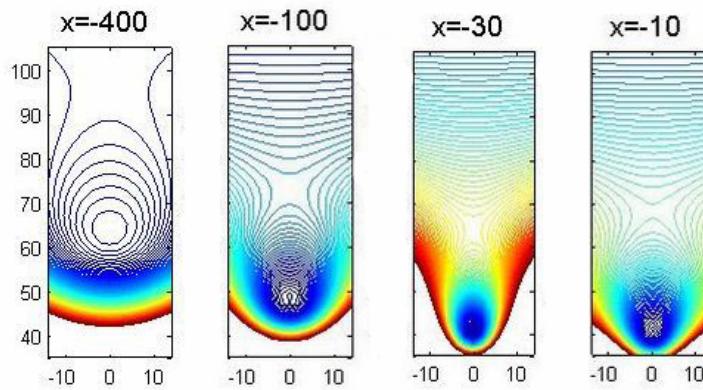
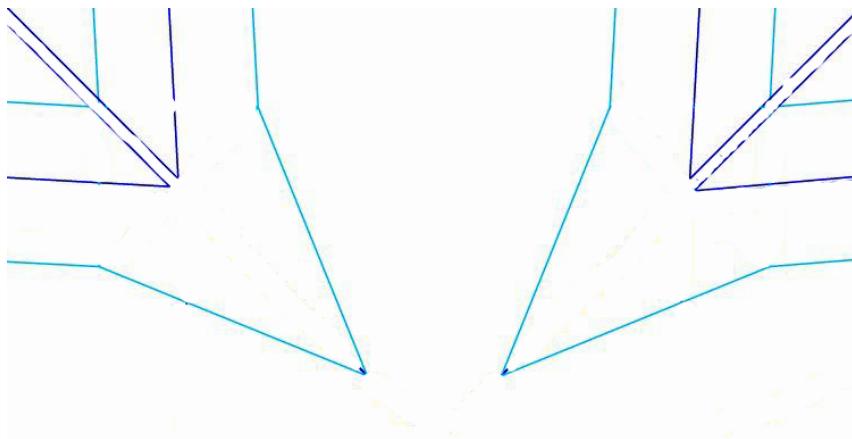
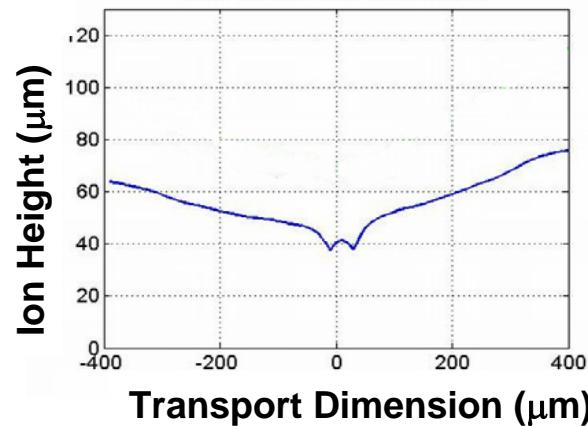
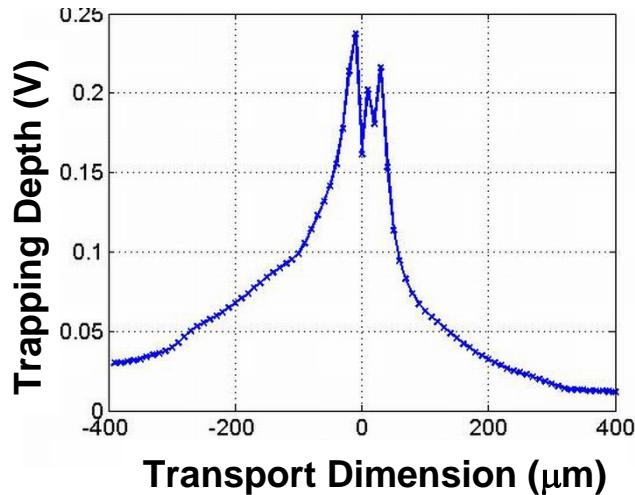
Revised Cross Trap



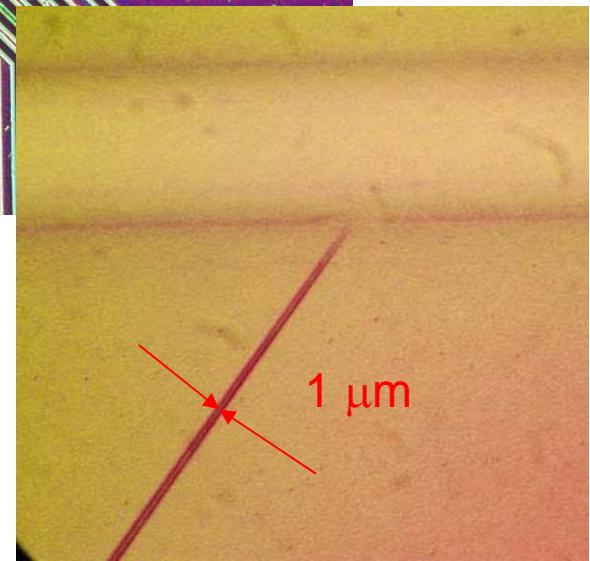
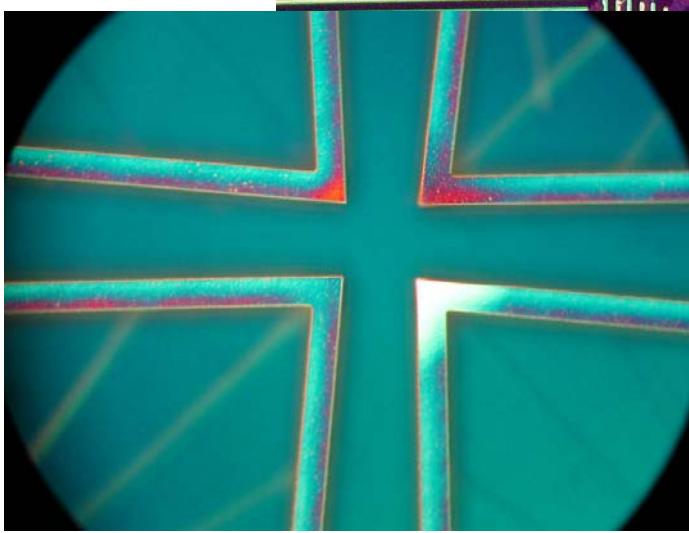
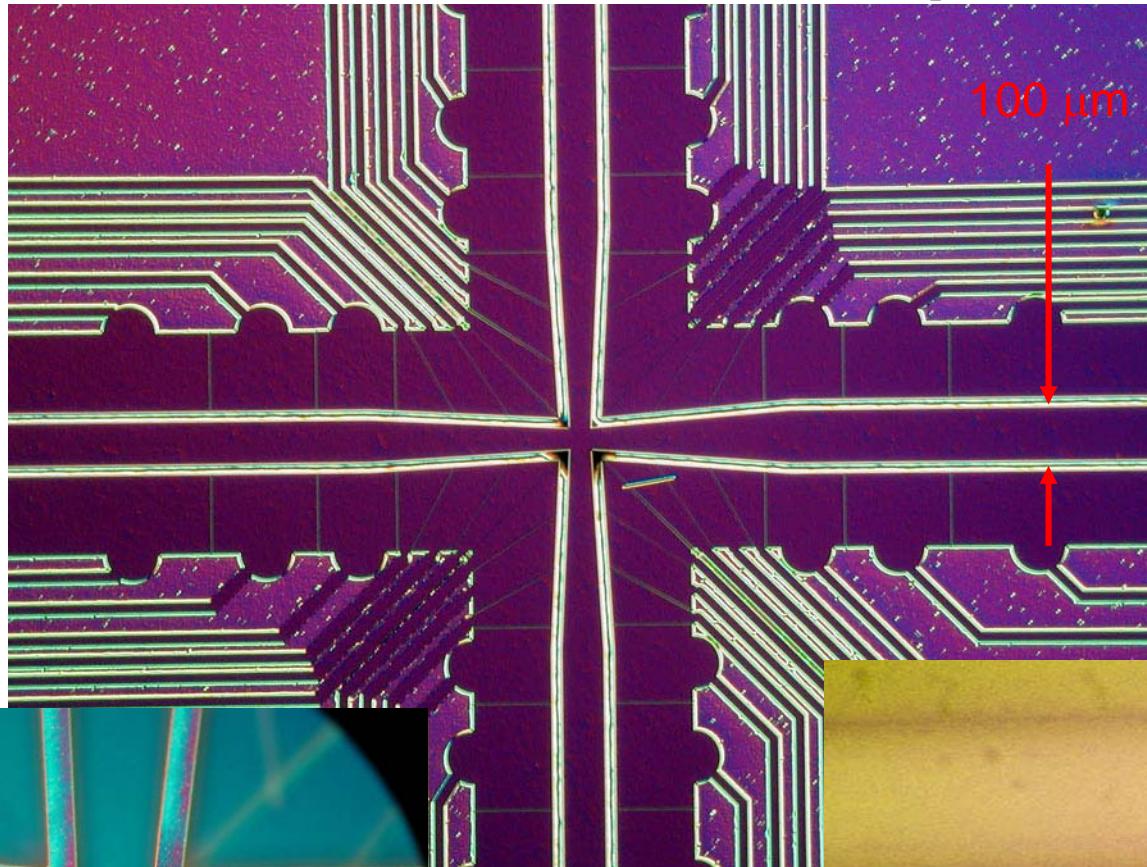
Present RF Cross



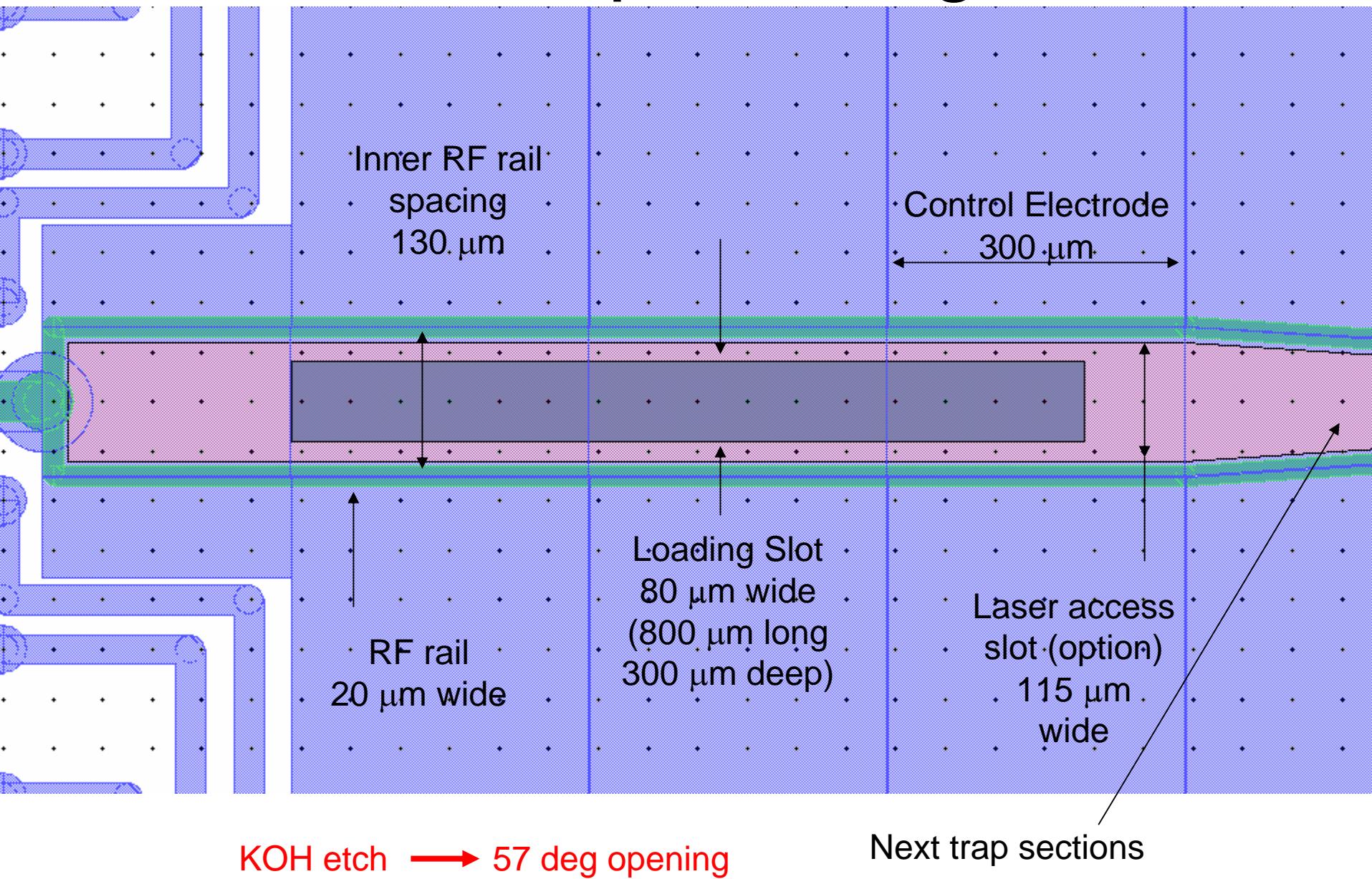
Enhanced RF Cross



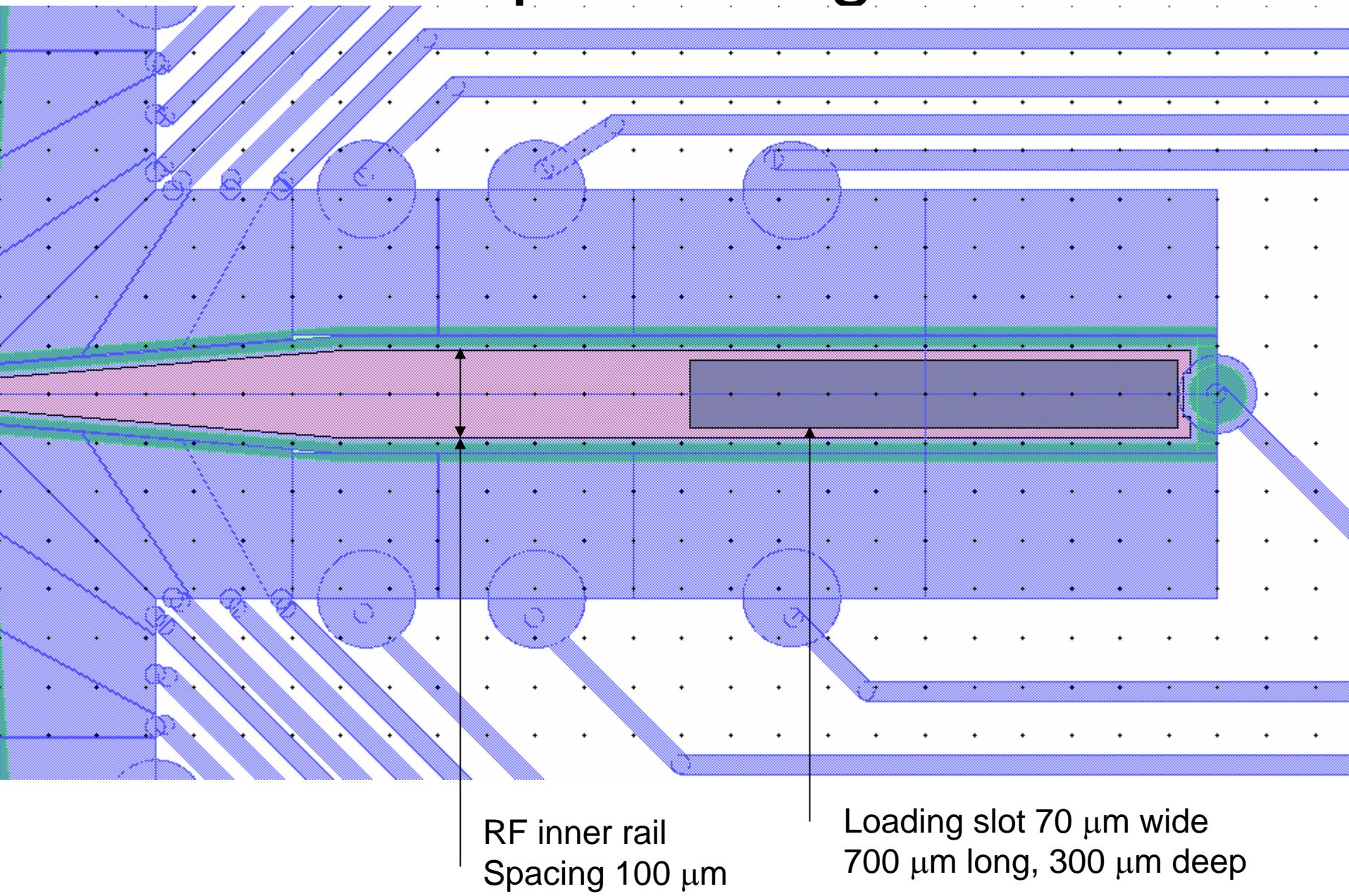
Revised X Trap



Linear Trap Loading Slot



X Trap Loading Slot



Summary



Planar ion traps

- Scalable vertical controls
- VLSI low T Process
 - ✓ Compatible with CMOS
- SMIDs (Single Instruction on Multiple Data)
 - ✓ Single gate laser - Multiple ion gates
 - ✓ Single cooling laser – Multiple ion traps
 - ✓ Single DAC – Multiple ion traps
- Materials and RF Q
- Ion cooling
- Micro-motion ?
- Anomalous heating ?
- Ion transport at Xs and Ts ?



ARDA

THANKS!!